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May 2016

Motion-SPM ™

FSB50825AB

Smart Power Module (SPM®)

Features

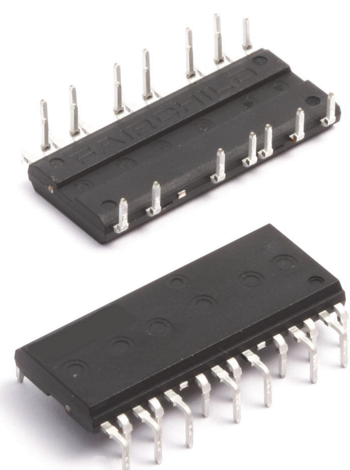
- 250V $R_{DS(on)}$=0.45Ω(max) 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min.
- HVIC temperature sensing
- Embedded bootstrap diode in the package
- RoHS compliant

Applications

- Three-phase inverter driver for small power ac motor drives

General Description

FSB50825AB is a tiny smart power module (SPM®) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB50825AB provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB50825AB is the best solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.



Absolute Maximum Ratings

Inverter Part (Each FRFET Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	DC Link Input Voltage, Drain-source Voltage of each FRFET		250	V
*I_{D25}	Each FRFET Drain Current, Continuous	T_C = 25°C	3.6	A
*I_{D80}	Each FRFET Drain Current, Continuous	T_C = 80°C	2.7	A
*I_{DP}	Each FRFET Drain Current, Peak	T_C = 25°C, PW < 100μs	9	A
*I_{DRMS}	Each FRFET Drain Current, Rms	T_C = 80°C, F_{PWM} < 20KHz	1.9	A_{rms}
*P_D	Maximum Power Dissipation	T_C = 25°C, For Each FRFET	14.2	W

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Units
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between V_B and V_S	20	V
V_{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ V_{CC}+0.3	V

Bootstrap Diode Part (Each Bootstrap diode Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Units
V_{RRMB}	Maixmum Repetitive Reverse Voltage		250	V
* I_{FB}	Forward Current	T_C = 25°C	0.5	A
* I_{FPB}	Forward Current (Peak)	T_C = 25°C, Under 1ms Pulse Width	1.5	A

Thermal Resistance

Symbol	Parameter	Conditions	Rating	Units
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each FRFET under inverter operating condition (Note 1)	8.8	°C/W

Total System

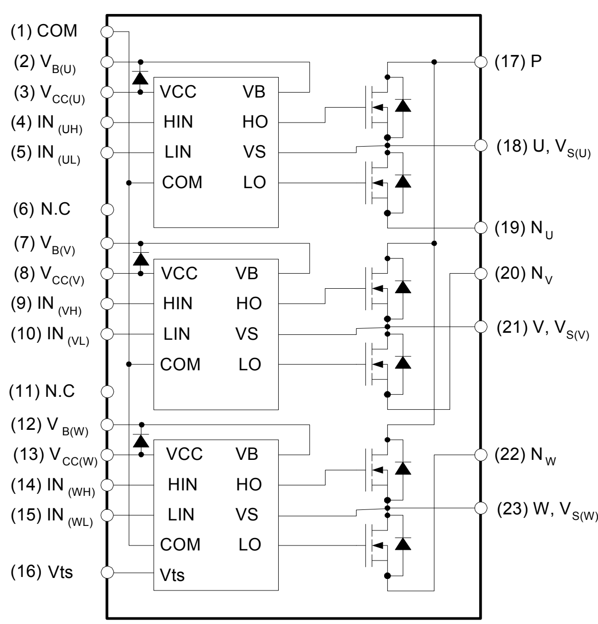
Symbol	Parameter	Conditions	Rating	Units
T_J	Operating Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-40 ~ 125	°C
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	V_{rms}

Note:

1. For the measurement point of case temperature T_C, please refer to Figure 4.
2. Marking " * " is calculation value or design factor.

Pin descriptions

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	N.C	N.C
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	N.C	N.C
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase High-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	V_{ts}	Output for HVIC temperature sensing
17	P	Positive DC–Link Input
18	U, $V_{S(U)}$	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving
19	N_U	Negative DC–Link Input for U Phase
20	N_V	Negative DC–Link Input for V Phase
21	V, $V_{S(V)}$	Output for V Phase & Bias Voltage Ground for High Side FRFET Driving
22	N_W	Negative DC–Link Input for W Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High Side FRFET Driving



Note:

Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside SPM®. External connections should be made as indicated in Figure 3

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Electrical Characteristics (T_J = 25°C, V_{CC}=V_{BS}=15V Unless Otherwise Specified)

Inverter Part (Each FRFET Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{IN}= 0V, I_D = 1mA (Note 1)	250	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{IN}= 0V, V_{DS} = 250V	-	-	1	mA
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{CC} = V_{BS} = 15V, V_{IN} = 5V, I_D = 2A	-	0.33	0.45	Ω
V_{SD}	Drain-Source Diode Forward Voltage	V_{CC} = V_{BS} = 15V, V_{IN} = 0V, I_D = -2A	-	-	1.2	V
t_{ON}	Switching Times	V_{PN} = 150V, V_{CC} = V_{BS} = 15V, I_D = 2A V_{IN} = 0V ↔ 5V, Inductive load L=3mH High- and low-side FRFET switching (Note 2)	-	950	-	ns
t_{OFF}			-	520	-	ns
t_{rr}			-	140	-	ns
E_{ON}			-	100	-	µJ
E_{OFF}			-	10	-	µJ
RBSOA	Reverse-bias Safe Operating Area	V_{PN} = 200V, V_{CC} = V_{BS} = 15V, I_D = I_{DP}, V_{DS}=BV_{DSS}, T_J = 150°C High- and low-side FRFET switching (Note 3)	Full Square			

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{QCC}	Quiescent V_{CC} Current	V_{CC}=15V, V_{IN}=0V	Applied between V_{CC} and COM	-	-	200	µA
I_{QBS}	Quiescent V_{BS} Current	V_{BS}=15V, V_{IN}=0V	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	-	-	100	µA
UV_{CCD}	Low-side Undervoltage Protection (Figure 8)	V_{CC} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV_{CCR}		V_{CC} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
UV_{BSD}	High-side Undervoltage Protection (Figure 9)	V_{BS} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV_{BSR}		V_{BS} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
V_{ts}	HVIC Temperature sensing voltage output	V_{CC}=15V, T_{HVIC}=25°C(Note 4)		600	790	980	mV
V_{IH}	ON Threshold Voltage	Logic High Level	Applied between IN and COM	-	-	2.9	V
V_{IL}	OFF Threshold Voltage	Logic Low Level		0.8	-	-	V

Bootstrap Diode Part (Each Bootstrap diode Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Forward Voltage	I_F = 0.1A, T_C = 25°C(Note 5)	-	2.5	-	V
t_{rrB}	Reverse Recovery Time	I_F = 0.1A, T_C = 25°C	-	80	-	ns

Note:

1. BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM®. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.
2. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applcations due to the effect of different printed circuit boards and wirings. Please see Figure 6 for the switching time definition with the switching test circuit of Figure 7.
3. The peak current and voltage of each FRFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 7 for the RBSOA test circuit that is same as the switching test circuit.
4. V_{ts} is only for sensing temperature of module and cannot shutdown MOSFETs automatically.
5. Built in bootstrap diode includes around 15Ω resistance characteristic. Please refer to Figure 2.

Recommended Operating Condition

Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P and N	-	150	200	V
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	12	13.5	15	V
V_{BS}	High-side Bias Voltage	Applied between V_B and V_S	12	13.5	15	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between IN and COM	3.0	-	V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	-	0.6	V
t_{dead}	Blanking Time for Preventing Arm-short	$V_{CC}=V_{BS}=12 \sim 15V$, $T_J \leq 150°C$	1.0	-	-	μs
f_{PWM}	PWM Switching Frequency	$T_J \leq 150°C$	-	15	-	kHz

Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
FSB50825AB	FSB50825AB	SPM23DD-21L	-	-	15

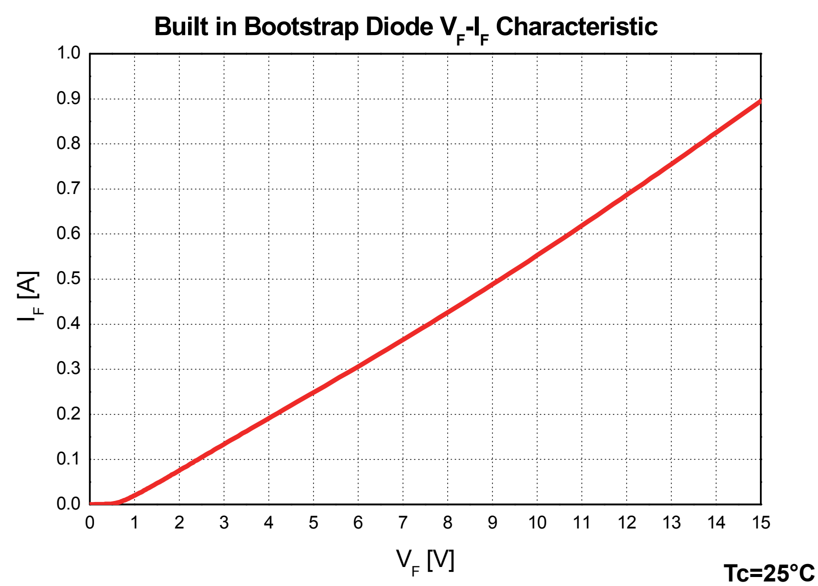
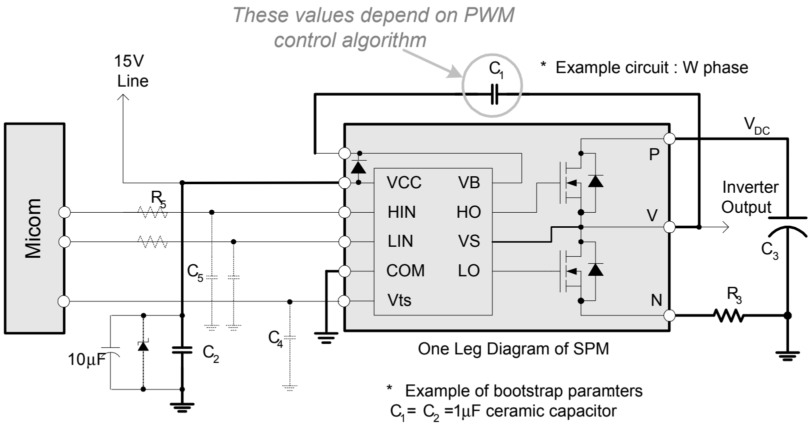


Figure 2. Built in Bootstrap Diode Characteristics(typ.)

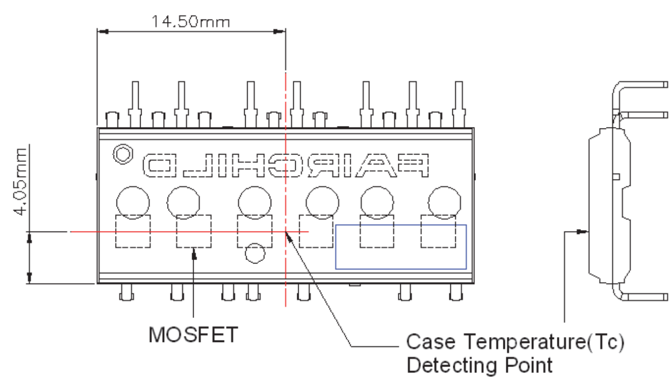


HIN	LIN	Output	Note
0	0	Z	Both FRFET Off
0	1	0	Low side FRFET On
1	0	V_{DC}	High side FRFET On
1	1	Forbidden	Shoot through
Open	Open	Z	Same as (0,0)

Note:

1. Parameters for bootsrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
2. RC coupling(R_5 and C_5) and C_4 at each input of SPM® and Micom (indicated as dotted lines) may be used to prevent improper signal due to surge noise.
3. Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as C_1, C_2 and C_3 should have good high-frequencycharacteristics to absorb high-frequency ripple current.

Figure 3. Recommended CPU Interface and Bootstrap Circuit with Parameters



Note:

Attach the thermocouple on top of the heatsink-side of SPM® (between SPM® and heatsink if applied) to get the correct temperature measurement.

Figure 4. Case Temperature Measurement

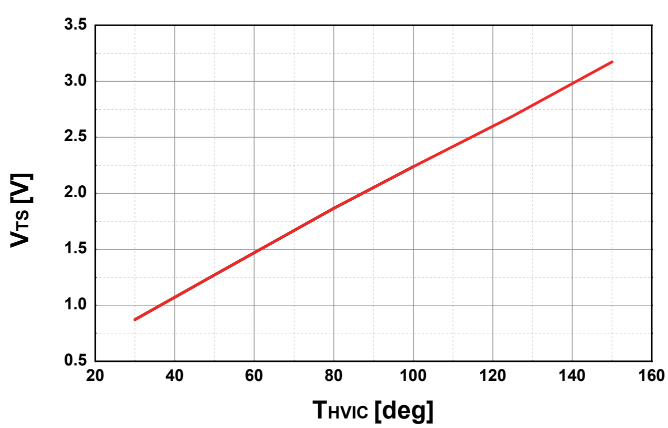
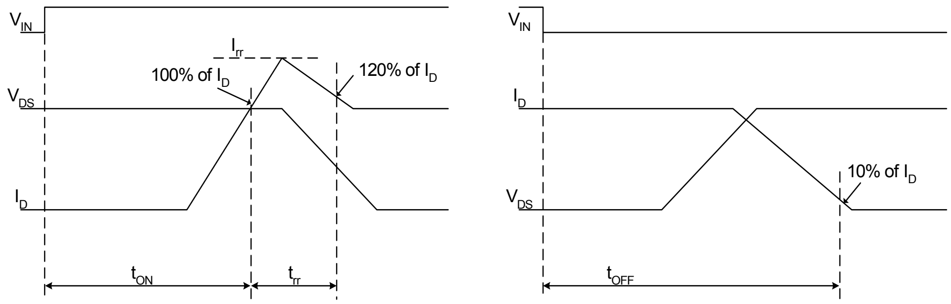


Figure 5. Temperature profile of V_{ts}(typ.)



(a) Turn-on (b) Turn-off

Figure 6. Switching Time Definition

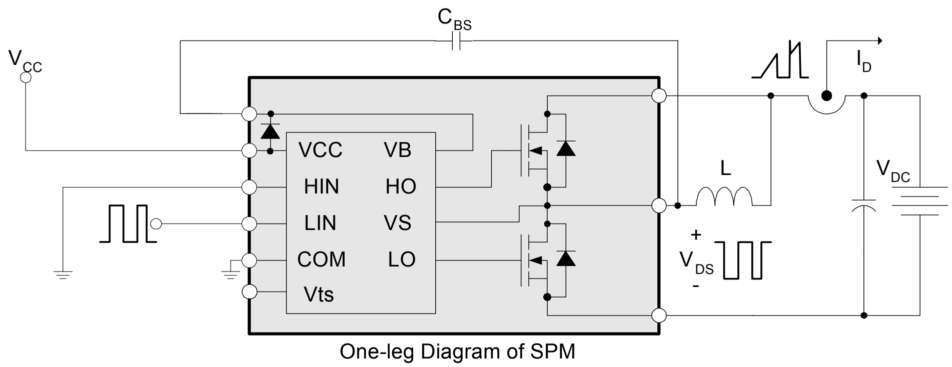


Figure 7. Switching and RBSOA(Single-pulse) Test Circuit (Low-side)

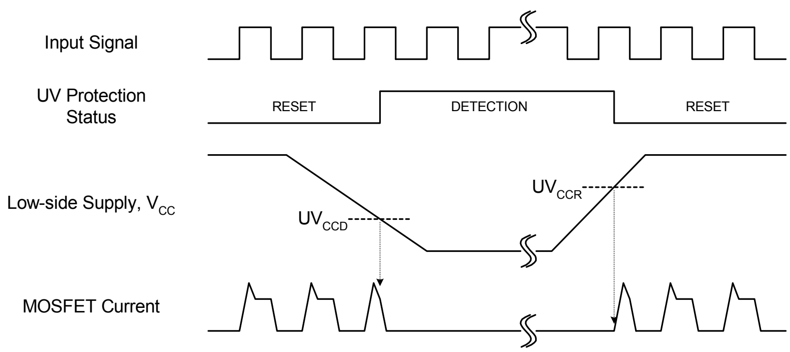


Figure 8. Undervoltage Protection (Low-side)

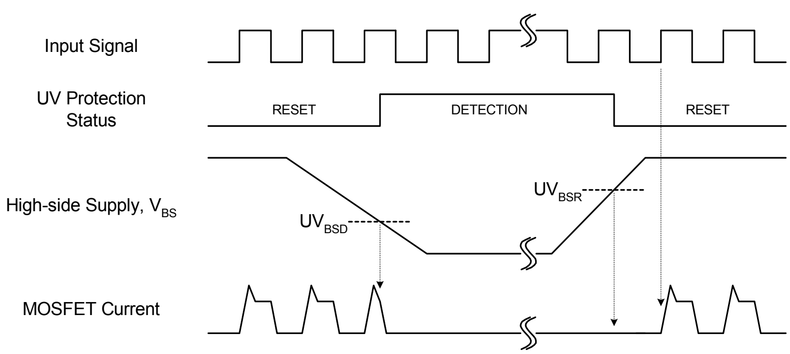
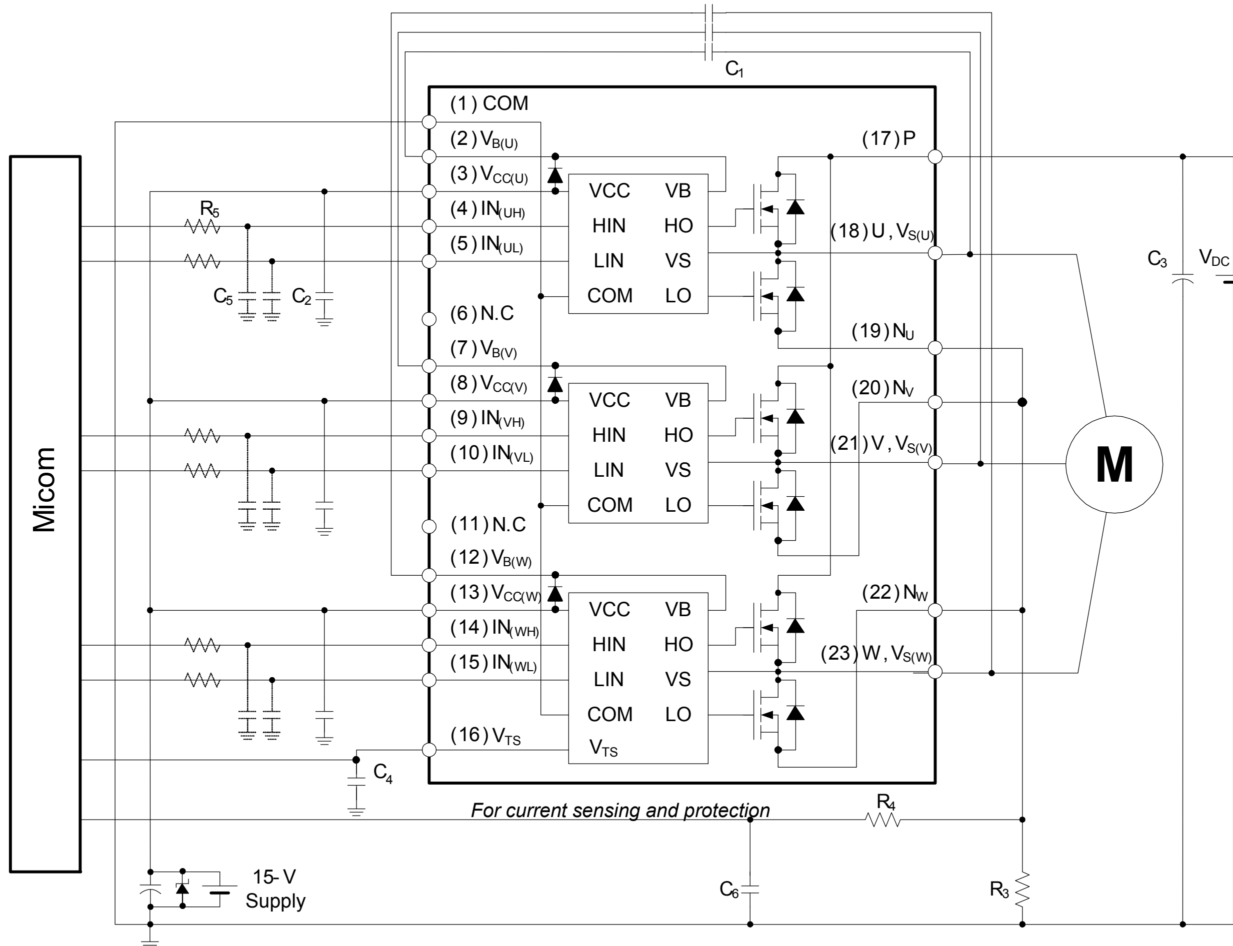


Figure 9. Undervoltage Protection (High-side)

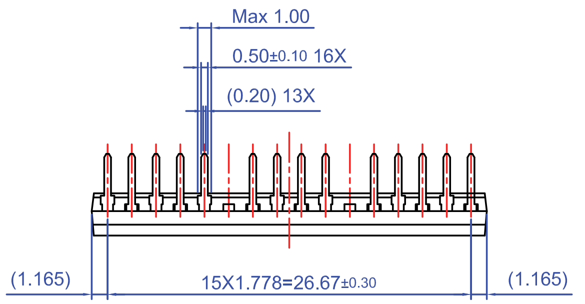


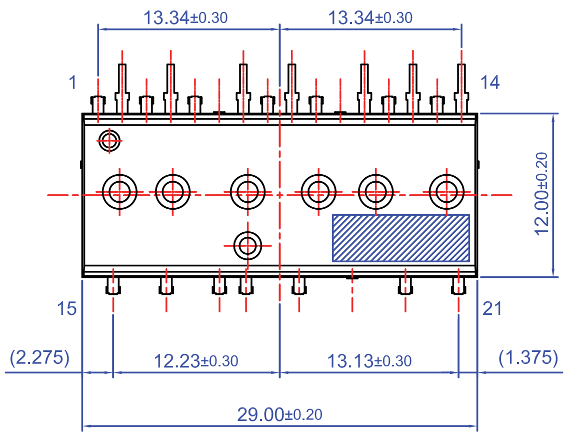
Note:

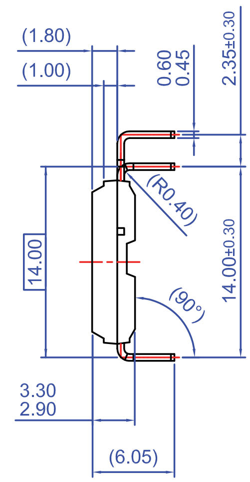
1. About pin position, refer to Figure 2.
2. RC coupling(R_5 and C_5, R_4 and C_6) and C_4 at each input of SPM® and Micom are useful to prevent improper input signal caused by surge noise.
3. The voltage drop across R_3 affects the low side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low side MOSFET. For this reason, the voltage drop across R_3 should be less than 1V in the steady-state.
4. Ground wires and output terminals, should be thick and short in order to avoid surge voltage and malfunction of HVIC.
5. All the filter capacitors shoud be connected close to SPM®, and they should have good characteristics for rejecting high-frequency ripple current.

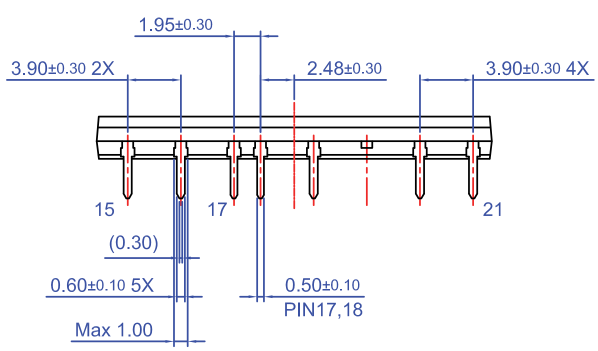
Figure 10. Example of Application Circuit

Detailed Package Outline Drawings









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